

## CLAIMS

What is claimed is:

- 1 1. A computer system, comprising:  
2 a processor;  
3 a system memory coupled to said processor;  
4 a bridge logic device coupled to said processor and said system memory and having a  
5 peripheral bus interface;  
6 a peripheral bus comprising a plurality of address lines and coupled to the peripheral bus  
7 interface of said bridge logic device, said peripheral bus capable of coupling together various  
8 peripheral devices;  
9 a keyboard coupled to said bridge logic device; and  
10 a logic device coupled to said peripheral bus that swaps two address lines when a  
11 peripheral bus cycle is run to a particular asserted address line.
- 1 2. The computer system of claim 1 wherein said peripheral bus comprises a PCI bus.
- 1 3. The computer system of claim 1 wherein said logic device comprises a PLD.
- 1 4. The computer system of claim 1 wherein said logic device swaps the two address lines  
2 when a peripheral bus configuration cycle is run.
- 1 5. The computer system of claim 4 wherein said logic device issues a retry to said bridge logic  
2 which, in response, issues a retry to said processor.

1 6. The computer system of claim 4 wherein said peripheral bus comprises a PCI bus and said  
2 logic device is a programmable logic device that detects a PCI configuration cycle run for one of  
3 the address lines comprising the PCI bus.

1 7. The computer system of claim 6 further comprising an electronically controlled switch  
2 coupled to and controlled by said programmable logic device, said switch receiving two PCI bus  
3 address lines.

1 8. The computer system of claim 6 wherein said programmable logic device switches the two  
2 PCI bus address lines when the programmable logic device detects a PCI bus configuration cycle  
3 targeted for one the two address lines so that the address line targeted by the PCI bus configuration  
4 cycle is electrically connected to the other of said two address lines.

1 9. The computer system of claim 7 further including a PCI device connected to said PCI bus  
2 that has its IDSEL input pin connected to one of said two address lines.

1 10. The computer system of claim 1 wherein said logic device swaps the two address lines only  
2 during a portion of the peripheral bus cycle and swaps the address lines back to their original state  
3 for the rest of the bus cycle.

1 11. A programmable logic device coupled to a system bus comprising a plurality of address  
2 lines, said programmable logic device having logic that detects configuration read or write cycle to

3 a particular system bus address line and, upon detecting a configuration read or write cycle to that  
4 particular address line, the programmable logic device asserts a control signal to an electronically-  
5 controlled switch to connect the particular system bus address line to another address line.

1 12. The programmable logic device of claim 11 wherein said programmable logic is coupled to  
2 a PCI bus comprising a plurality of AD lines and said programmable logic device detects a PCI bus  
3 configuration read or write cycle to AD16.

1 13. The programmable logic device of claim 11 wherein said programmable logic is coupled to  
2 a PCI bus comprising a plurality of AD lines and said programmable logic device asserts the  
3 control signal during a portion of said configuration cycle and deasserts the control signal during  
4 the rest of the configuration cycle.

1 14. The programmable logic device of claim 11 wherein programmable logic device issues a  
2 retry signal upon detecting the configuration read or write cycle to the said particular address line.

1 15. A method of avoiding a conflict on a system bus having a plurality of address lines during a  
2 configuration cycle, comprising:

- 3 (a) detecting a configuration cycle associated with a particular system bus address line;  
4 (b) changing the state of a switch so that one of said address lines is connected to another of  
5 said address lines; and  
6 (c) changing the state of the switch back to its state before (b) was performed.

1 16. The method of claim 15 wherein the system bus comprises a PCI bus and (a) comprises  
2 detecting a PCI bus configuration cycle associated one of said PCI bus address lines.

1 17. The method of claim 16 wherein (b) includes changing the state of the switch during only a  
2 portion of the PCI bus configuration cycle.

1 18. The method of claim 17 further including issuing a retry after detecting a configuration  
2 cycle associated with the particular system bus address line and before changing the state of the  
3 switch in (b).

1 19. The method of claim 15 wherein (a) includes detecting a configuration cycle associated  
2 with a system bus address line that conflicts with a configuration cycle intended for a device  
3 connected to said system bus.

1 20. The method of claim 15 in which (b) includes connecting an address line that is not  
2 hardwired as a chip select signal to an address line that is hardwired as a chip select signal.

1 21. The method of claim 15 wherein (b) occurs only during an address phase of the  
2 configuration cycle.

1 22. The method of claim 21 wherein the system bus is a PCI bus having address lines  
2 AD[31::0] and (b) includes connecting AD16 to AD11.

1 23. A computer system, comprising:  
2 a processor;  
3 a bridge logic device coupled to said process and a system bus that comprises a plurality of  
4 address lines;  
5 at least one system bus peripheral device connected to said system bus;  
6 an electronically-controlled switch connected to at least one of said system bus address  
7 lines; and  
8 a means for detecting a system bus configuration cycle associated with a certain system bus  
9 address line and, upon detecting the configuration cycle associated with the certain system bus  
10 address line, asserting a control signal to said switch to connect the certain system bus address line  
11 to another of the system bus address lines.